

**IN THE CLAIMS:**

1.-17. (Canceled)

18. (Original) A device, comprising:

a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said transistor being comprised of a gate electrode, said bulk substrate being doped with a dopant material at a first concentration level; and

first, second and third doped regions formed in said bulk substrate, said first, second and third doped regions being comprised of a dopant material that is the same type as said bulk substrate dopant material, said first, second and third doped regions having a greater concentration level of dopant material than said first concentration level, said first doped region being substantially aligned with said gate electrode and vertically spaced apart from said second and third doped regions.

19. (Original) The device of claim 18, wherein said transistor is comprised of at least one of an NMOS and PMOS device.

20. (Original) The device of claim 18, wherein said buried oxide layer is comprised of silicon dioxide and has a thickness ranging from approximately 5-50 nm.

21. (Original) The device of claim 18, wherein said active layer is comprised of silicon and has a thickness of approximately 5-30 nm.

22. (Original) The device of claim 18, wherein said gate electrode is comprised of polysilicon and has a thickness of approximately 100-150 nm.

23. (Original) The device of claim 18, wherein said gate electrode has a thickness and wherein said first doped region is vertically spaced apart from said second and third doped regions by a distance that corresponds approximately to said thickness of said gate electrode.

24. (Original) The device of claim 18, wherein said bulk substrate is doped with a P-type dopant material at a concentration level of approximately  $10^{15}$  ions/cm<sup>3</sup> and said first, second and third doped regions are doped with a P-type dopant material at a dopant concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>.

25. (Original) The device of claim 18, wherein said bulk substrate is doped with an N-type dopant material at a concentration level of approximately  $10^{15}$  ions/cm<sup>3</sup> and said first, second and third doped regions are doped with an N-type dopant material at a dopant concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>.

26. (Original) The device of claim 18, wherein said first, second and third doped regions each have a thickness of approximately 10-50 nm.

27. (Original) The device of claim 18, wherein each of said second and third doped regions has an inner edge that is approximately aligned with respect to said gate electrode.

28. (Original) The device of claim 18, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

29. (Original) The device of claim 18, wherein said second and third doped regions each have an upper surface that is positioned below an interface between the buried oxide layer and the bulk substrate by a distance that corresponds approximately to a thickness of the gate electrode.

30. (Original) The device of claim 18, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections.

31. (Original) A device, comprising:

a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said transistor being comprised of a gate electrode having a thickness, said bulk substrate being doped with a dopant material at a first concentration level; and

first, second and third doped regions formed in said bulk substrate, said first, second and third doped regions being comprised of a dopant material that is the same type as said bulk substrate dopant material, said first, second and third doped regions

having a greater concentration level of dopant material than said first concentration level and at least a concentration level of approximately  $10^{16}$  ions/cm<sup>3</sup>, said first doped region being substantially aligned with said gate electrode and vertically spaced apart from said second and third doped regions by a distance that corresponds approximately to said thickness of said gate electrode.

32. (Original) The device of claim 31, wherein said transistor is comprised of at least one of an NMOS and PMOS device.

33. (Original) The device of claim 31, wherein said buried oxide layer is comprised of silicon dioxide and has a thickness ranging from approximately 5-50 nm.

34. (Original) The device of claim 31, wherein said active layer is comprised of silicon and has a thickness of approximately 5-30 nm.

35. (Original) The device of claim 31, wherein said gate electrode is comprised of polysilicon and has a thickness of approximately 100-150 nm.

36. (Original) The device of claim 31, wherein said bulk substrate is doped with a P-type dopant material at a concentration level of approximately  $10^{15}$  ions/cm<sup>3</sup> and said first, second and third doped regions are doped with a P-type dopant material at a dopant concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>.

37. (Original) The device of claim 31, wherein said bulk substrate is doped with an N-type dopant material at a concentration level of approximately  $10^{15}$  ions/cm<sup>3</sup> and said first, second and third doped regions are doped with an N-type dopant material at a dopant concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>.

38. (Original) The device of claim 31, wherein said first, second and third doped regions each have a thickness of approximately 10-50 nm.

39. (Original) The device of claim 31, wherein each of said second and third doped regions has an inner edge that is approximately aligned with respect to said gate electrode.

40. (Original) The device of claim 31, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

41. (Original) The device of claim 31, wherein said second and third doped regions each have an upper surface that is positioned below an interface between the buried oxide layer and the bulk substrate by a distance that corresponds approximately to the thickness of the gate electrode.

42. (Original) The device of claim 31, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections.

43.-76. (Canceled)

77. (New) A device, comprising:

a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer comprised of silicon, said transistor being comprised of a gate electrode having a thickness, said bulk substrate being doped with a dopant material at a first concentration level, said buried oxide layer being comprised of silicon dioxide; and

first, second and third doped regions formed in said bulk substrate, said first, second and third doped regions being comprised of a dopant material that is the same type as said bulk substrate dopant material, said first, second and third doped regions having a thickness of approximately 10-50 nm and a greater concentration level of dopant material than said first concentration level and at least a concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>, said first doped region being substantially aligned with said gate electrode and vertically spaced apart from said second and third doped regions by a distance that corresponds approximately to said thickness of said gate electrode.

78. (New) The device of claim 77, wherein said transistor is comprised of at least one of an NMOS and PMOS device.

79. (New) The device of claim 77, wherein said buried oxide layer has a thickness ranging from approximately 5-50 nm.

80. (New) The device of claim 77, wherein said active layer has a thickness of approximately 5-30 nm.

81. (New) The device of claim 77, wherein said gate electrode is comprised of polysilicon and has a thickness of approximately 100-150 nm.

82. (New) The device of claim 77, wherein said bulk substrate is doped with a P-type dopant material at a concentration level of approximately  $10^{15}$  ions/cm<sup>3</sup> and said first, second and third doped regions are doped with a P-type dopant material at a dopant concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>.

83. (New) The device of claim 77, wherein said bulk substrate is doped with an N-type dopant material at a concentration level of approximately  $10^{15}$  ions/cm<sup>3</sup> and said first, second and third doped regions are doped with an N-type dopant material at a dopant concentration level of at least approximately  $10^{16}$  ions/cm<sup>3</sup>.

84. (New) The device of claim 77, wherein each of said second and third doped regions has an inner edge that is approximately aligned with respect to said gate electrode.

85. (New) The device of claim 77, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

86. (New) The device of claim 77, wherein said second and third doped regions each have an upper surface that is positioned below an interface between the buried oxide layer and the bulk substrate by a distance that corresponds approximately to the thickness of the gate electrode.

87. (New) The device of claim 77, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections.